REMARKS

Claims 1, 3, 5-11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,131,141(Ravid) in view of U.S. Patent No. 6,556,769 (Akahane et al.), U.S. Patent No. 5,237,466 (Glaser et al.) and Logic and Computer Design Fundamentals, by Mano and Kime.

The Examiner's rejection is respectfully traversed.

The Applicant's invention directed to a duplicator for recording medium. The duplicator includes a source recording medium, a source DMAC, a source FIFO buffer, a multiplexer, a plurality of target FIFO buffers, a plurality of target DMACs, and a plurality of target recording mediums. The data of the source recording medium are transmitted to the source FIFO buffer through the source DMAC. The data of the source FIFO are transmitted to a plurality of the target FIFO buffers through the multiplexer. The data of the target FIFO buffers are transmitted to the target recording medium through the target DMAC.

The modern IDE HDD can support transfer several protocols, as defined in the ATA specification, including PIO mode, Multi-word DMA mode and Ultra DMA mode, etc. The PIO mode is the first generation of all and it could support 3.3 MB/sec initially in 1985 and improved to 16 MB/sec later on. The PIO mode required heavy CPU usage. Subsequently, the Multi-word DMA was created to remove CPU load. However, the speed was still limited to 16 MB/sec. For both PIO and Multi-word DMA modes, the data are strobed with the rising edge of the command from host. To improve the transfer speed, Ultra-DMA mode was created to use both rising and falling edges to strobe data. As a result, the Ultra-

DMA mode can support up to 100 or 133MB/sec.

The inventor of this invention has built IDE HDD duplicators since 1989. The PC-based duplicator included multiple IDE interface cards (first generation duplicator). Attached hereto are the figures to clarify the distinctions of the invention. Fig. 1 shows a block diagram of first generation duplicator, wherein each IDE card is assigned to a different address. The data were read from the source HDD, and then were written to the target HDDs one by one. All work was done by a CPU of the PC. The timing diagrams of reading and writing operations in PIO mode are shown in Fig. 2. The timing diagrams of reading data from the source HDD and writing data into the target HDDs as a duplicator are shown in Fig. 3. The timing diagrams of reading data from the source HDD and reading data from the target HDDs as a comparator are shown in Fig. 4.

The operation sequences as a duplicator look like:

Reading from source HDD (first cycle)

Writing to target 1 HDD (second cycle)

Writing to target 2 HDD (third cycle)

.....

Writing to target n HDD (n+1th cycle)

On the other hand, the operation sequences as a comparator look like:

Reading from source HDD (first cycle)

Reading from target 1 HDD (second cycle)

Reading from target 2 HDD (third cycle)

.....

Reading from to target n HDD (n+1th cycle)

Therefore, for N target HDDs, it would take (1+N) cycles to copy and (1+N) cycles to compare.

To speed up the operation, the inventor of this application improved the interface cards to let it write the same data to multiple target HDDs in one cycle (second generator duplicator). The inventor adds a circuit to generate one write command to all target HDDs. The timing diagrams of reading data from the source HDD and writing data into the target HDDs as a duplicator are shown in Fig. 5.

The sequence as a duplicator would look like:

Reading from source HDD (first cycle)

Writing to multiple target HDDs (second cycle)

Accordingly, it takes only two cycles to copy.

The inventor of this application made an improvement by incorporating one step to replace a plurality of steps (third generation duplicator), wherein the read command strobe is used to generate write command strobes for all target HDDs, and the data read from the source HDD are fed to the target HDDs through the system data bus. The timing diagrams of reading data from the source HDD and writing data into the target HDDs as a duplicator are shown in Fig. 6.

Therefore, it takes only once cycle to copy:

Reading from the source HDD + writing to multiple target HDDs (one cycle).

Next, the inventor of this application added comparators to the interface card of each target HDD to speed up comparing operation. The timing diagrams of reading data from the source HDD and reading data from the target HDDs as a comparator are shown in Fig.

7.

Reading from the source HDD + reading from multiple target HDDs and comparing (one cycle).

It should be noted that only PIO mode can be (or Multi-word mode may be) used with this direct data passing through method by using switch and control signal modifiers because the read/write data strobes are generated by the host, i.e. the duplicator. The design of Ravid'141 is similar to that of the inventor's third generation duplicator which can not apply to Ultra-DMA mode.

As a new protocol, the Ultra-DMA mode breaks this model, because the date strobe is generated by the HDD during reading. In the previous method, there is no memory in the data path as claimed in the '141 patent. The '141 patent can not handle the data bursts from the HDD of new protocol. The important technical features of this invention are explained in detail in the following description.

The inventor of this application uses FIFO and DMAC combined to handle the data to/from HDD to support the Ultra-DMA mode for further speed up the operations. The data and control signal of every HDD are independent each other. So, it can do both burst-in and burst-out. The timing diagrams of reading data from the source HDD and writing data into the target HDDs as a duplicator which applies the Ultra DMA mode are shown in Fig. 8, wherein DSTROBE and DD are sent by the source HDD, and HSTROBE and DD are sent by host. Ultra-DMA mode is created to use both rising and falling edges to strobe data.

The block diagrams of a duplicator and comparator in this invention are shown in Figs. 9 and 10, respectively. This invention controls the data flow between FIFOs. The DMAC can also generate data strobe to handle PIO mode and Multi-word DMA mode. Each DMAC generates its own timing with data to/from the FIFO. Therefore, the setup/hold timing margin will be better than the '141 patent, which will be impacted by a propagation delay or jitter distortion in the data switch and control signal switch from the central control signal generator. Also, it should be noted that, as shown in Figs. 9 and 10, DSTROBE and DD are sent by the source HDD, the '141 patent can not apply to the Ultra-DMA mode since it is not possible to determine the time when DSTROBE and DD are sent by the source HDD. Accordingly, only the Applicant's invention can apply to the Ultra-DMA mode for supporting up to 100 or 133 MB/sec. Obvious, this invention possesses novelty and inventive step over '141 patent.

The Akahane et al.'769' patent uses a RAM to store data, and the HDD used in the '769 patent is an extension memory like a virtual memory. The DMAC and FIFO used in the '769 patent are different from this application in purpose and control manner. The DMAC in this application is not used for transferring data without processor intervention. Instead, the DMAC in this application is used for generating a control signal for HDD and FIFO.

The multiplexer in this application is used as a constant/random data generator which is used for HDD test or erase. On the other hand, the multiplexer in the '141 patent is connected to a printer port for outer data.

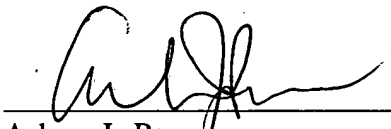
The Glaser et al. '466 patent relates to programmably controlling spindle synchronization and phase among disk drives. The '466 patent is irrelevant to this

application.

In view of the foregoing, the Applicant believes that the amended claims and the claims dependent there from are in proper form. The Applicant respectfully contends that Ravid'141, Akahane et al.'769, Glaser et al.'466 and Logic and Computer Design Fundamentals, by Mano and Kime, do not anticipate the claimed invention under the provisions of 35 U.S.C. §103(a). Thus, claims 1, 3, and 5-11 should be considered patently distinguishable over the prior art of record and in proper form.

The application is now considered to be in condition for allowance, and an early indication of same is earnestly solicited

Respectfully submitted,



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